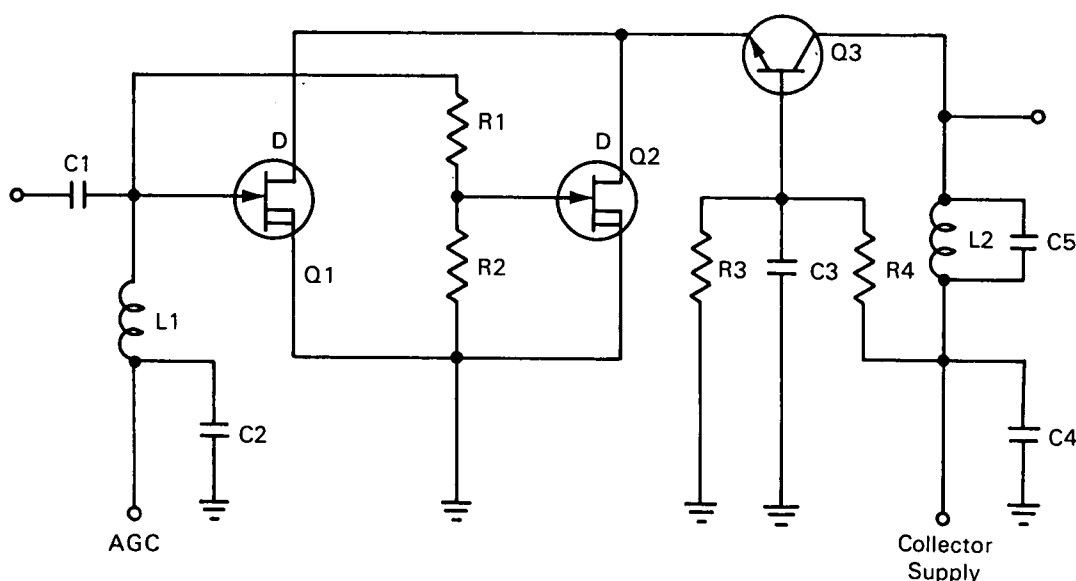


NASA TECH BRIEF



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Field Effect Transistor (FET) Circuit for Variable Gain Amplifiers



The problem:

To design an amplifier that combines improved input and output impedances with relatively large signal handling capability and an immunity from the usual adverse effects of automatic gain control. While the remote cutoff pentode and some integrated circuits operate in this fashion, they each suffer from major deficiencies. The pentode requires the use of considerable heater power and demands high dc potentials, while integrated circuits lack signal handling capability and are subject to impedance variations with gain control.

The solution:

A circuit that combines the above described advantages through the use of two FETs with sources

and drains in parallel plus a resistive divider for signal and bias to either of the gate terminals.

How it's done:

C1 couples the ac signal into the circuit and L1 provides a high impedance to the ac signal and a low impedance path for the AGC potential. C2, C3 and C4 are bypass capacitors to provide low impedance ac signal paths. R3 and R4 provide a bias for the base of transistor Q3. L2 and C5 form a tuned resonant circuit which is a load impedance at the ac operating frequency. R1 and R2 form a resistive divider that divides the ac signal and AGC potential applied to the gate of Q1 and applies the divided signals to the gate of Q2. The two FETs Q1 and Q2 with drains and sources in parallel and their gates

(continued overleaf)

tied together through the resistive divider R1 and R2, produce the remote cutoff feature that makes the circuit perform like a remote cutoff vacuum tube. At low values of AGC bias both FETs Q1 and Q2 contribute to the forward transfer admittance. Since the signal is attenuated, Q2 does not contribute as much to the forward transfer admittance under low values of AGC bias as Q1 does. As the bias is increased, Q1 approaches cutoff more rapidly than Q2 because the bias applied to Q2 is also divided by R1 and R2. As Q1 approaches cutoff, the forward transfer admittance of the circuit becomes controlled by Q2. The AGC bias required to cutoff Q2 is larger than that required to cutoff Q1 by a factor determined by R1 and R2. By selecting the ratio of R1 and R2, the dc transfer characteristic of the FETs can be optimized for a smooth transition of the transfer characteristic or for remoteness of cutoff. Since the signal is divided by the resistors, larger signals may be used as Q2 approaches cutoff for the same amount of distortion in the drain current.

The grounded base transistor Q3 provides a low impedance drain load for Q1 and Q2. The emitter impedance is comparatively low. This factor reduces the reverse energy transfer from drain-to-gate of Q1 and Q2 and therefore, by reducing the Miller effect, reduces input impedance variations as a function of

AGC. The reduction of this Miller effect is a very important feature because it virtually eliminates input impedance variations as a function of AGC voltage. This feature is especially important in RF and IF amplifiers where input impedance variations can alter the bandwidth and center frequency of the previous stage. The output impedance of Q3 remains high and minimizes the variations in damping across the load tuned circuit.

Note:

No further documentation is available. Inquiries may be directed to:

Technology Utilization Officer
Goddard Space Flight Center
Greenbelt, Maryland 20771
Reference: B69-10322

Patent status:

Inquiries about obtaining rights for the commercial use of this invention may be made to NASA, Code GP, Washington, D.C. 20546.

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